PCI Express® Architecture PHY Test Specification Revision 4.0

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1.Introduction

This document provides test descriptions for PCI Express electrical testing. It is relevant for anyone building add-in cards or system boards to the PCI Express Card Electromechanical Specification 4.0. This specification does not describe the full set of PCI Express tests and assertions for these devices.

In particular, devices must also meet the requirements and tests described in the latest versions of the following documents as well as any other tests provided by the PCI-SIG:

PCI Express Architecture Configuration Space Test Specification

Platform BIOS Test Considerations for the PCI Express Architecture

PCI Express Architecture Link Layer Test Specification

PCI Express Architecture Transaction Layer Test Specification

1.1. Coverage

This document covers items in the PCI Express Card Electromechanical Revision 4.0 or Base Specification Revision 4.0 that apply to 16 GT/s, 8.0 GT/s, 5.0 GT/s and 2.5 GT/s signaling. 5.0 GT/s signaling requirements described in the PHY Electrical Test Consideration Revision 2.0 document apply to PCIe 2.0 devices that support 5.0GT/s and 2.5 GT/s signaling. 2.5 GT/s signaling requirements described in the PHY Electrical Test Considerations Revision 1.1 document apply to PCIe2.0, PCIe 1.1 and PCIe 1.0a devices that support 2.5 GT/s signaling.

2

2. Test Descriptions

2.1. Add-in Card Transmitter Signal Quality

This test is run on all card electromechanical (CEM) form factor add-in cards. The test verifies that the signaling of the system at 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s with all specified transmitter equalization values meets eye diagram and other jitter requirements.

Starting Configuration

Overview of Test Steps

2.1.1. Add-in Card Transmitter Electrical Compliance Test for 2.5 GT/s and 5.0 GT/s

2.1.2. Add-in Card Transmitter Electrical Compliance Test for 8.0 GT/s

2.1.3. Add-in Card Transmitter Electrical Compliance Test for 16.0 GT/s

2.2. Add-in Card Transmitter Preset Test

This test is run on all card electromechanical form factor add-in cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the add-in card produces the correct transmitter equalization values for each preset in the set of 11 presets.

Starting Configuration

Overview of Test Steps

2.2.1. Add-in Card Transmitter Preset Test for 8.0 GT/s

2.2.2. Add-in Card Transmitter Preset Test for 16.0 GT/s

2.3. Add-in Card Transmitter Initial TX EQ Test

This test is run on all card electromechanical form factor add-in cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the add-in card will start with the correxT TX EQ preset requested through the protocol.

Starting Configuration

Overview of Test Steps

2.3.1. Add-in Card Transmitter Initial TX EQ test for 8.0 GT/s

2.3.2. Add-in Card Transmitter Initial TX EQ test for 16.0 GT/s

2.4. Add-in Card Transmitter Link Equalization Response Test

This test is run on all card electromechanical form factor add-in cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the add-in card will respond correctly to transmitter equalization commands sent via the link protocol.

Starting Configuration

Overview of Test Steps

2.4.1. Add-in Card Transmitter Link Equalization Response Test for 8.0 GT/s

2.4.2. Add-in Card Transmitter Link Equalization Response Test for 16.0 GT/s

2.5. System Board Transmitter Signal Quality

This test is run on all card electromechanical form factor system boards. The test verifies that the signaling of the system at 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s with all specified transmitter equalization values meets eye diagram and other jitter requirements.

Starting Configuration

Overview of Test Steps

2.5.1. System Board Transmitter Electrical Compliance Test for 2.5 GT/s and 5.0 GT/s

2.5.2. System Board Transmitter Electrical Compliance Test for 8.0 GT/s

2.5.3. System Board Transmitter Electrical Compliance Test for 16.0 GT/s

2.6. System Board Transmitter Preset Test

This test is run on all card electromechanical form factor system boards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system board produces the correct transmitter equalization values for each preset in the set of 11 presets.

Starting Configuration

Overview of Test Steps

2.6.1. System Board Transmitter Preset Test for 8.0 GT/s

2.6.2. System Board Transmitter Preset Test for 16.0 GT/s

2.7. System Board Transmitter Link Equalization Response Test

This test is run on all card electromechanical form factor system boards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system will respond correctly to transmitter equalization commands sent via the link protocol.

Starting Configuration

Overview of Test Steps

2.7.1. System Board Transmitter Link Equalization Response Test for 8.0 GT/s

2.7.2. System Board Transmitter Link Equalization Response Test for 16.0 GT/s

2.8. Add-in Card Receiver Jitter Tolerance Test

This test is run on all card electromechanical form factor add-in cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the add-in card can function normally in systems with jitter near the specification allowed limits and does not exceed the allowed receiver error rate in loopback mode.

Starting Configuration

Overview of Calibration Steps

2.8.1. Add-in Card Receiver Jitter Tolerance Test at 8.0 GT/s

2.8.2. Add-in Card Receiver Jitter Tolerance Test at 16.0 GT/s

2.9. System Receiver Jitter Tolerance Test

This test is run on all Card Electromechanical (CEM) form factor system boards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system can function normally with an add-in card with jitter near the specification allowed limits and does not exceed the allowed receiver error rate in loopback mode.

Starting Configuration

Overview of Calibration Steps

2.9.1. System Receiver Jitter Tolerance Test for 8.0 GT/s

2.9.2. System Receiver Jitter Tolerance Test for 16.0 GT/s

2.10. Add-in Card Receiver Link Equalization Test

This test is run on all card electromechanical form factor add-in cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the add-in card will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately.

Starting Configuration

Overview of Calibration Steps

2.10.1. System Receiver Jitter Tolerance Test for 8.0 GT/s

2.10.2. System Receiver Jitter Tolerance Test for 16.0 GT/s

2.11. Add-in Card Receiver Link Equalization Test

This test is run on all Card Electromechanical (CEM) form factor system boards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system will correctly negotiate with its link partner to adust the partner's transmitter equalization appropriately.

2.11.1. System Receiver Link Equalization Test for 8.0 GT/s

2.11.2. System Receiver Link Equalization Test for 16.0 GT/s

2.12. Add-in Card PLL Bandwidth

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card PLL bandwidth and peaking are within the limits allowed by the PCI Express specifications.

Starting Configuration

Overview of Test Steps

2.13. Add-in Card PCB Impedance (informative)

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card TX and RX path PCB differential trace impedance is in the range required by the PCI Express 3.0 Card Electromechanical Specification.

The differential impedance of the Tx and Rx lanes is checked with a TDR or equivalent to verify that the measured impedance of the PCB trace only (package is excluded) is within the CEM specification.

2.14. System Board PCB Impedance (Informative)

This test is run on all card electromechanical form factor system boards. The test verifies that the system board TX and RX path PCB differential trace impedance is in the range required by the PCI Express 3.0 Card Electromechanical Specification.

The differential impedance of some or all of the Tx and Rx lanes is checked with a TDR or equivalent to verify that the measured impedance of the PCB trace only is within specification.

A

3. Appendix A: Getting into Loopback

In order to perform receiver tolerance tests the product under test must first be trained and directed to enter the Loopback state. This is done by taking the product through the state machine from Detect via Polling and Configuration to the Loopback state using the protocol as specified in PCI Express Base Specification, Rev 2.0.

3.1. Loopback Training

The state transitions needed to get the device under test into loopback mode are pictured in **Error! Reference source not found.** below:

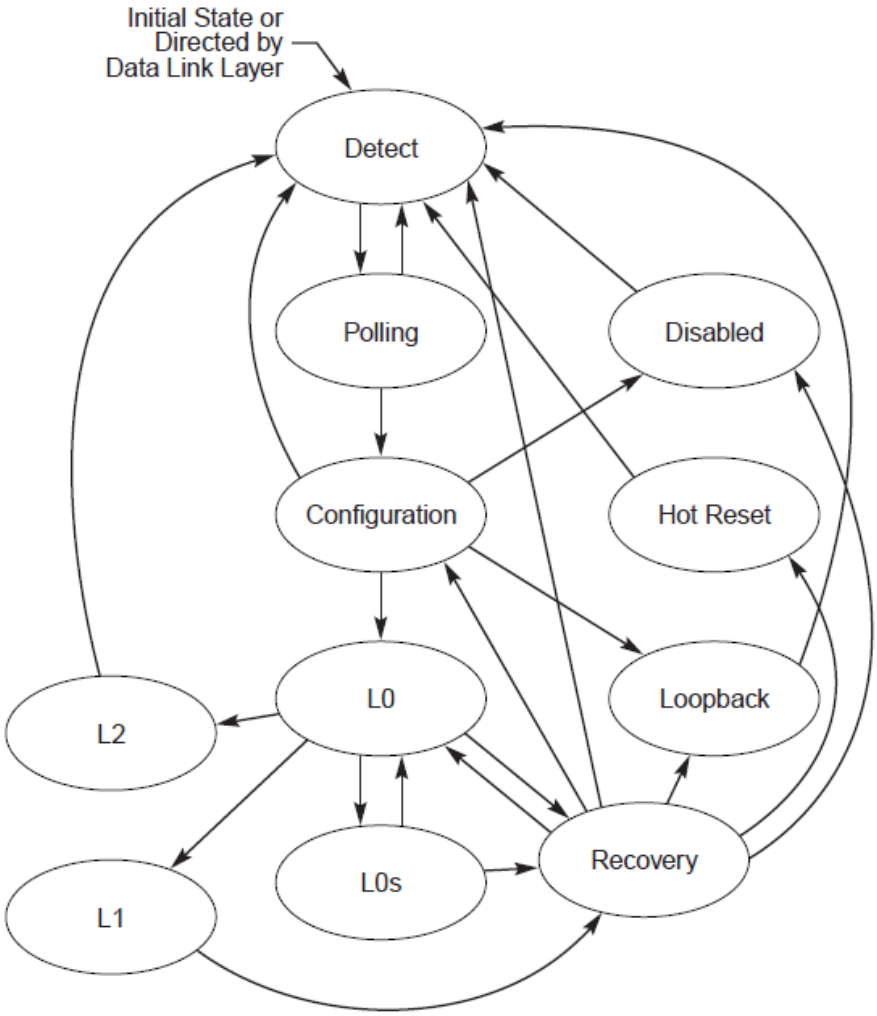


Figure 1: Main State Diagram for Link Training and Status State Machine

3.2. Step by Step Sequence

The following sequence of steps will cause the device under test to enter loopback state:

1. Start sending TS1 with PAD (K23.7) which takes the product into the Polling.Active state.

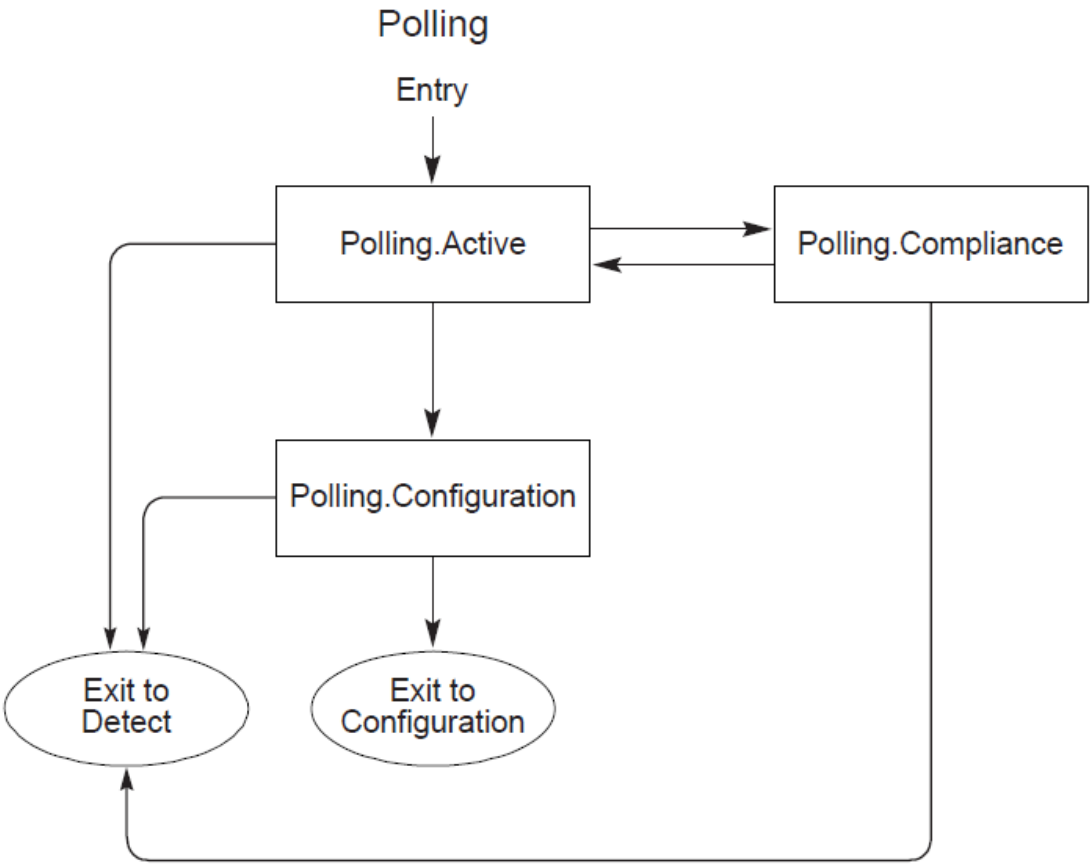


Figure 2: Polling Substate Machine

2. Polling.Configuration is reached after >1024 TS1 have been transmitted and 8 consecutive TS1 or TS2 with Pad or Loopback bit asserted have been received.
3. The Configuration state is entered after 8 consecutive TS2 with Pad have been received and 16 TS2 have been transmitted after 1 TS2 has been received.
4. Speed negotiation is initiated by sending TS1 at 2.5 GT/s advertising the supported speeds.
5. Electrical idle for more than 1 ms allows the product to adjust to the requested speed unless the requested speed is 2.5 GT/s.
6. Two consecutive TS1 at the requested speed with Loopback bit asserted takes the product to the Loopback state.

3.3. Loopback training at 2.5 GT/s

The sequence necessary to cause a device under test to enter loopback at a data rate of 2.5 GT/s is shown in figure 3 below:

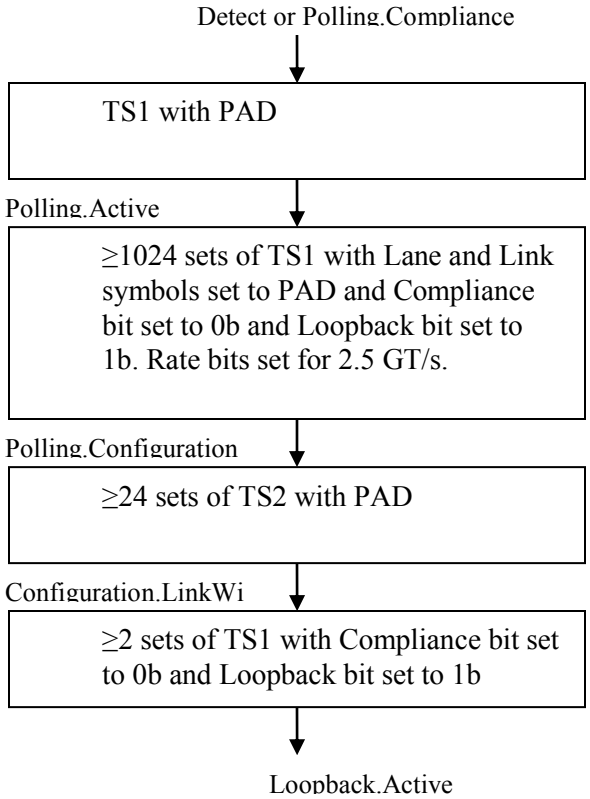


Figure 3: 2.5 BT/s Loopback Training Sequence

3.4. Loopback training at 5.0 GT/s

The sequence necessary to cause a device under test to enter loopback at a data rate of 5.0 GT/s is shown in figure 4 below:

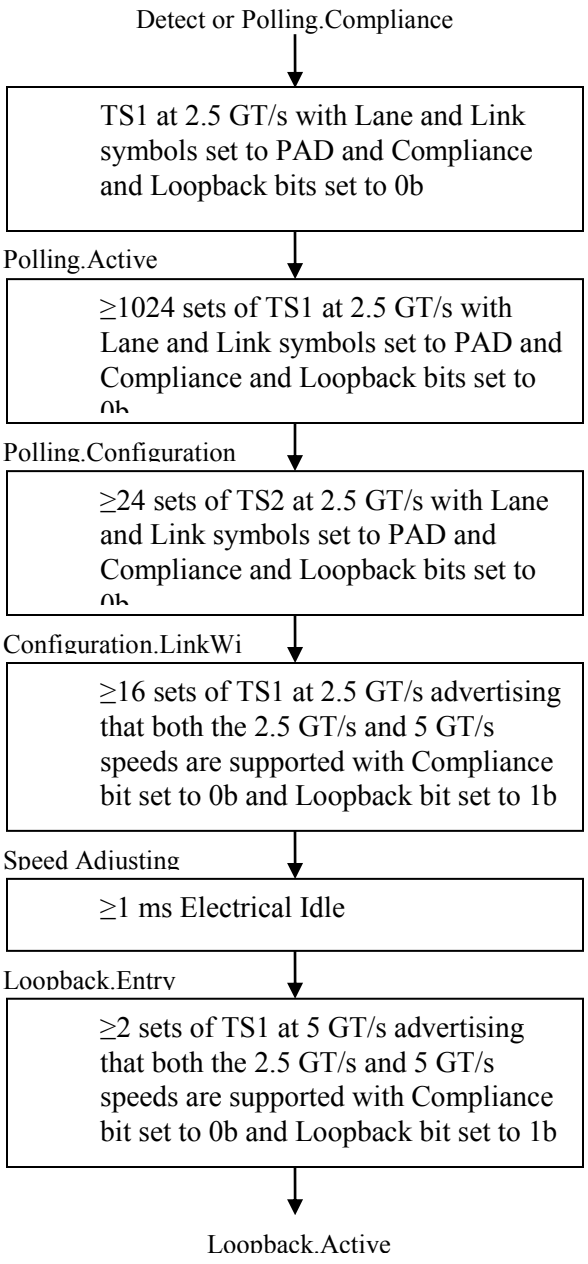


Figure 4: 5.0 GT/ s Loopback Training Sequence

3.5. Loopback training at 8.0 GT/s

The sequences that will be used to cause a device under test to enter loopback through the configuration link state and through the recovery link state at a data rate of 8.0 GT/s are specified in the PCI Express 3.0 Link Test Specification..

B

4. Appendix B: Transmitter Signaling Analysis

The process of analyzing transmitter output to determine the signal quality and, ultimately, the ability of a particular transmitter to operate with any receiver that complies with the receiver specification is an intricate process. While the Dual Dirac method used in this analysis is well documented elsewhere, it is useful to describe this analysis technique as used for transmitter testing here.

4.1. Outline of Tx signal analysis

Within the context of PCI Express, transmitter electrical compliance is computed by analyzing a waveform captured using a high-speed, real time oscilloscope. Because of the high frequency nature of the signal being analyzed, the oscilloscope must have a bandwidth of at least 6 Ghz and a sample rate of at least 20 GS/s (50 ps sample interval) for 2.5 GT/s signaling and a bandwidth of at least 12 Ghz and a sample rate of at least 40 GS/s (25 ps sample interval) for 5.0 GT/s and 8.0 GT/s signaling and a bandwidth of at least 24 Ghz and a sample rate of at least 80 GS/s (12.5 ps sample interval) for 16.0GT/s.

The captured waveform is optionally conditioned by a specified test channel and specified receiver equalization (CTLE and DFE). The resulting waveform is then analyzed for timing jitter and minimum and maximum signal amplitude.

Timing analysis is based on a specified target Unit Interval (UI) and, when doing random jitter (Rj) and deterministic jitter (Dj) separation, timing uncertenty extrapolated to a Bit Error Rate (BER) than can be significantly greater than the BER computed directly from the measured data.

Signal amplitude analysis is based on the measured waveform amplitude as modified by any specified waveform conditioning (test channel embedding and Rx equalization) and related to timing defined by the specified target UI.

4.1.1. Input Waveform Conditioning

Three different forms of waveform conditioning can be applied to the input waveform:

4.1.1.1 Channel Embedding

The channel is defined by S-Parameters. The channel description is read in and stored internally. When a waveform is presented for processing, the waveform is converted to the frequency domain then multiplied with the channel description. The result of the multiplication is converted back to the time domain.

The waveform is input as two single-ended acquisitions or a single differential acquisition and output as a single, differential waveform.

4.1.1.2 CTLE Equalization

Continuous Time Linear Equalization (CTLE) is performed in a similiar manner to Channel Embedding. The input waveform is transformed into the frequency domain. The CTLE parameters (AC/DC gain, one zero frequency and two pole frequencies) are used to define an equivalent frequency domain response and the input waveform is convolved with the CTLE response. The result of the convolution is converted back to the time domain.

Multiple CTLE parameter sets can be specified. The waveform resulting from each CTLE filter then has DFE applied. The optimal CTLE (and, if specified, DFE) parameter set is determined by examining the resulting transition and non-transition eye heights and widths for each set of CTLE parameters. Once the optimal CTLE (and DFE, if specified) parameter set has been determined, it is applied to the entire waveform.

4.1.1.3 DFE Equalization

Decision Feedback Equalization (DFE) is performed strictly in the time domain. The eye area is used to find the optimal DFE tap value between – 30 and + 30 mV (inclusive). Once the taps are known, each sample point of the input waveform is modified according to the tap values and the state (logic 0 or logic 1) of the waveform at each tap location.

4.1.2. Crossover and Interval Determination

Once the input waveform conditioning has been performed, the input waveform is analyzed to determine the time at which the signal crosses the zero Volts threshold. The crossover time is determined using linear interpolation between the two sample points closest to the zero crossing.

The interval between successive crossovers is computed by subtracting the crossover time at the beginning of the interval from the crossover time at the end of the interval: $Interval_n = Crossover_{n+1} – Crossover_n$. Information allowing a given interval to be traced back to its location within the input waveform is retained.

In most cases, (all cases except when the input waveform is a toggle pattern) the input waveform will contain multi-bit intervals. To meet the analysis requirements, the multi-bit intervals need to be replaced with multiple single bit intervals. The period of each added interval is merely the period of the original, multi-bit interval divided by the number of unit intervals represented.

Since this step is where the bit length of each interval is determined, any pattern checks that have been specified are performed at this time.

4.1.3. Time Interval Error (or Phase Jitter) Determination

The jitter per edge and the subsequent Time Interval Error (TIE) are computed based on the clock period for each unit interval in the input data. For single port measurements (as used in Add-In Card analysis) a single clock value is computed for the entire data record. For dual port analysis (as used in System Board analysis) the clock for each unit interval in the data reacord is computed from the supplied clock waveform. These methods are described below.

4.1.3.1 Single Port (Add-In Card) Jitter Determination

No explicit clock information is provided for single port analysis so the clock must be determined from the data waveform. Two methods are available for doing this, least squares fit and mean interval.

4.1.3.2 Least Suqares Fit Clock Interval Method

The least squares fit method plots the interval duration on the Y axis against the interval on the X axis. The least squares fit line is computed and the slope of this line is used as the unit interval period for jitter determination.

4.1.3.3 Mean Clock Interval Method

The mean interval method merely finds the mean of all the intervals and uses this value as the unit interval period for jitter determination.

4.1.3.4 Single Port Data Waveform Phase Jitter Computation

The jitter at each interval is found by subtracting the unit interval period (as computed above) from each interval. It is important to note that the resulting jitter value can be either positive (interval is greater than unit interval) or negative (interval is less than unit interval).

Finally, this jitter data is converted into phase jitter or the Time Interval Error (TIE) by accumulation; that is, the jitter at each unit interval is summed to give the TIE at that UI: $TIE_0 = J_0$, $TIE_n = TIE_{n-1} + J_n$.

4.1.3.5 Dual Port (System Board) Jitter Determination

For dual port analysis, the system clock is captured simultaneously with the data. Both the clock waveform and the data waveform are input to the analysis software and the data waveform is processed as described above in sections 4.1.1 through 4.1.2.

The clock waveform is processed in a similar maner, but without any waveform conditioning. Further, in general, the crossover times of only the rising edge of the clock waveform are interpolated. The resulting crossover periods (from rising edge to rising edge of the clock signal) are then interpolated to the correct number of unit intervals.

At this point, there is an array of unit interval values for the data and an array of unit interval value for the clock.

4.1.3.6 Phase-Locked Loop (PLL) Filter of Clock Jitter

Several different PLL filter values are specified to constrain the effect of the transmit and receive PLLs on the clock. For each specified filter value, the clock values are filtered according to each set of PLL filter parameters. The jitter values are computed for each filter specified and the total jitter (Tj) is used to determine which results to retain. The largest Tj found is retained as the result for all clock filter values.

4.1.3.7 Clock to Data Skew

Even though the clock waveform is captured simultaneously with the data waveform, there may be delay between the clock and data waveforms due to different routing on the system board.

The CEM spec defines a maximum for this skew. To compensate for this possible skew, the analysis is done at three different values of clock to data skew:

1. Clock delayed by maximum allowed amount with respect to the data.
2. No delay introduced between clock and data.
3. Data delayed by maximum allowed amount with respect to the clock.

Obviously, any delay must be an integer number of unit intervals so the number of unit intervals closest the the specified maximum skew is used to offset the clock and data values.

As with the PLL filter values, the total jitter is computed for all three delay combinations and the worst case Tj is retained as the final result. If there are three filters specified there will be three skew cases for each filter thus the algorithm to find the total jitter will be executed nine times in all.

4.1.3.8 Dual Port Data Waveform Phase Jitter Computation

The jitter at each interval is found by subtracting the clock interval from the data interval. The clock interval has been filtered (as noted in section 4.1.3.6 above) and clock to data skew has been applied (as noted in section 4.1.3.7 above). The phase jitter or Time Interval Error (TIE) is computed as described for the single port data waveform jitter in section 4.1.3.4 above.

4.1.4. Jitter Determination

The phase jitter, whether computed using the single port or dual port method, is used to compute the total jitter and, by application of the Dual Dirac method, the deterministic jitter.

4.1.4.1 Phase Jitter High Pass Filter

A high pass filter is applied to the phase jitter based on parameters specified. The filter can be a brick wall filter or a simple first or second order filter. The cut-off frequency, damping factor (for second order filters) and brickwall floor value (for brick wall filters) are specified for this filter.

4.1.4.2 Jitter Metrics

At this point, the total jitter for each unit interval represented in the input waveform is known. Jitter metrics such as maximum peak-to-peak jitter are computed and saved for display later.

4.1.4.3 Dual Dirac Fitting

With the suitably filtered jitter values available, first the Probability Distribution Function (PDF) then the left and right Cumulative Distribution Functions are computed. The PDF is found by forming a histogram of the jitter values around zero; the number of bins to be used in the histogram is supplied as a parameter to this function. The range of jitter values determines the size of each bin in picoseconds.

The cumulative distribution functions are found by accumulating the PDF from one end to the other. The left side CDF is generated by by accumulating the PDF from left to right (index 0 through index *n*), the right side CDF is gnereated by accumulating the PDF from the right to the left (index *n* through 0).

The left and right CDF values are converted to Q space using the complementary inverse error function. Specifically, the CDF is multiplied by two, converted by the complementary inverse error function then multiplied by the square root of two. The complementary inverse error function has the interesting property of mapping a Gaussian distribution into a straight line. Thus a Gaussian can be extrapolated in Q space merely by extending a straight line. This is done for both left and right cumulative distribution functions using a slope (Rj) computed from the frequency domain phase jitter.